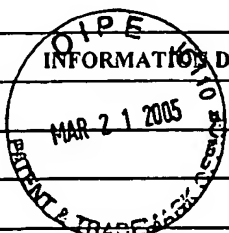


<sup>6</sup>Applicant is to place a check mark here if English language Translation is attached.





PTO/SB/08A (Substitute for form 1449/PTO)		Attorney Docket No.: 023-0031
		Application No.: 10/729,843
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		First Named Inventor: Luca G. Fasoli et al.
		Filing Date: December 5, 2003
		Group Art Unit: 2824
		Examiner Name: <del>Pho-M-Luu</del> VTN
Sheet 1 of 5		Date Submitted: March 15, 2005



U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. <sup>1</sup>	Document Number Number-Kind Code <sup>2</sup> (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	
VTN	AA	4,142,176	02-27-1979	Dozier		
	AB	4,543,594	09-24-1985	Mohsen et al.		
	AC	4,602,354	07-22-1986	Craycraft et al.		
	AD	4,868,616	09-19-1989	Johnson et al.		
	AE	5,197,027	03-23-1993	Challa		
	AF	5,301,144	04-05-1994	Kohno		
	AG	5,412,493	05-02-1995	Kunii et al.		
	AH	5,429,968	07-04-1995	Koyama		
	AI	5,473,563	12-05-1995	Suh et al.		
	AJ	5,568,421	10-22-1996	Aritome		
	AK	5,621,683	04-15-1997	Young		
	AL	5,644,533	07-01-1997	Lancaster et al.		
VTN	AM	5,703,382	12-30-1997	Hack et al.		
FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document Country Code <sup>3</sup> -Number <sup>4</sup> -Kind Code <sup>5</sup> (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
VTN	AN	JA 62-142363	06-25-1987			
	AO	JA 62-155568	07-10-1987			
	AP	JA-2001-358237	12-26-2001			
VTN	AQ	JA-2002-280467	09-27-2002			
Examiner Signature: <i>[Signature]</i>			Date Considered: 1/7/06			

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup>Applicant's unique citation designation number (optional).

<sup>2</sup>See Kinds Codes of USPTO Patent Documents at [www.uspto.gov](http://www.uspto.gov) or MPEP 901.04.

<sup>3</sup>Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3)

<sup>4</sup>For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document.

<sup>5</sup>Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible.

<sup>6</sup>Applicant is to place a check mark here if English language Translation is attached.

PTO/SB/08A (Substitute for form 1449/PTO)	Attorney Docket No.: 023-0031
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT	First Named Inventor: Luca G. Fasoli et al.
(Continuation Sheet)	Filing Date: December 5, 2003
	Group Art Unit: 2824
	Examiner Name: Pho M. Luu VTN
Sheet 2 of 5	Date Submitted: March 15, 2005

U.S. PATENT DOCUMENTS
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VTN	AR	5,715,194	02-03-1998	Hu	
	AS	5,751,012	05-12-1998	Wolstenholme et al.	
	AT	5,814,853	09-29-1998	Chen	
	AU	5,835,396	11-10-1998	Zhang	
	AV	5,898,615	04-27-1999	Chida	
	AW	5,923,587	07-13-1999	Choi	
	AX	5,926,415	07-20-1999	Shin	
	AY	5,940,321	08-17-1999	Takeuchi et al.	
	AZ	5,978,265	11-02-1999	Kirisawa et al.	
	BA	6,034,882	03-07-2000	Johnson et al.	
	BB	6,055,180	04-25-2000	Gudesen et al.	
	BC	6,107,658	08-22-2000	Itoh et al.	
VTN	BD	6,185,122 B1	02-06-2001	Johnson et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document Country Code <sup>3</sup> -Number <sup>4</sup> -Kind Code <sup>5</sup> (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
	BE					
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	BG					
	BH					
Examiner Signature		Pho M. Luu		Date Considered	1/7/06	

PTO/SB/08A (Substitute for form 1449/PTO)	Attorney Docket No.: 023-0031
	Application No.: 10/729,843
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	First Named Inventor: Luca G. Fasoli et al.
(Continuation Sheet)	Filing Date: December 5, 2003
	Group Art Unit: 2824
	Examiner Name: Pho M. Lma VTN
Sheet 3 of 5	Date Submitted: March 15, 2005

U.S. PATENT DOCUMENTS
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VTN	BI	6,188,611 B1	02-13-2001	Endoh et al.	
	BJ	6,291,836	09-18-2001	Kramer et al.	
	BK	6,307,807 B1	10-23-2001	Sakui et al.	
	BL	6,326,269 B1	12-04-2001	Jeng et al.	
	BM	6,373,746 B1	04-16-2002	Takeuchi et al.	
	BN	6,434,053	08-13-2002	Fujiwara	
	BO	6,445,613	09-03-2002	Nagai	
	BP	6,469,933 B2	10-22-2002	Choi et al.	
	BQ	6,473,328	10-29-2002	Mercaldi	
	BR	6,477,077	11-05-2002	Okazawa	
	BS	6,490,194	12-03-2002	Hoenigschmid	
	BT	6,498,747	12-24-2002	Gogl et al.	
NTN	BU	6,512,703 B2	01-28-2003	Sakui et al.	

FOREIGN PATENT DOCUMENTS						
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT	First Named Inventor: Luca G. Fasoli et al.
(Continuation Sheet)	Filing Date: December 5, 2003
	Group Art Unit: 2824
	Examiner Name: Pho M. Luu
Sheet 4 of 5	Date Submitted: March 15, 2005

U.S. PATENT DOCUMENTS
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VTN	BZ	6,515,888	02-04-2003	Johnson et al.	
	CA	6,545,898	04-08-2003	Scheuerlein	
	CB	6,567,312 B1	05-20-2003	Torii et al.	
	CC	6,597,609 B2	07-22-2003	Chevallier	
	CD	6,611,453	08-26-2003	Ning	
	CE	6,614,688 B2	09-02-2003	Jcong et al.	
	CF	6,618,292 B2	09-09-2003	Sakui	
	CG	6,621,743 B2	09-16-2003	Ogane	
	CH	6,822,903 B2	11-23-2004	Scheuerlein et al.	
	CI	6,849,905 B2	02-01-2005	Ilkbahar et al.	
	CJ	6,856,572 B2	02-15-2005	Scheuerlein et al.	
	CK	6,859,410 B2	02-22-2005	Scheuerlein et al.	
VTN	CL	US RE. 35,838	07-07-1998	Momodomi et al.	

FOREIGN PATENT DOCUMENTS						
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	CO					
	CP					
Examiner Signature		[Signature]		Date Considered	VTN	

PTO/SB/08A (Substitute for form 1449/PTO)	Attorney Docket No.: 023-0031
	Application No.: 10/729,843
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	First Named Inventor: Luca G. Fasoli et al.
(Continuation Sheet)	Filing Date: December 5, 2003
	Group Art Unit: 2824
	Examiner Name: Pho-M. Luu VTN
Sheet 5 of 5	Date Submitted: March 15, 2005

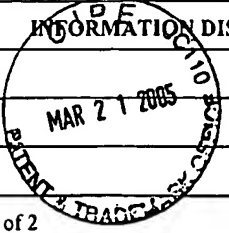
**U.S. PATENT DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Document Number Number-Kind Code <sup>2</sup> (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
VTN	CQ	US-2002/0021587 A1.	02-21-2002	Sakui et al	
	CR	US-2002/0028541 A2	03-07-2002	Lee et al.	
	CS	US-2003/0155582 A1	08-21-2003	Mahajani et al.	
	CT	US-2004/0124415	07-01-2004	Walker et al.	
	CU	US-2004/0124466	07-01-2004	Walker et al.	
	CV	US-2004/0125629 A1	07-01-2004	Scheuerlein et al.	
	CW	US-2004/045024 A1	07-29-2004	Chen et al.	
	CX	US-6,108,238	08-2000	Nakamura et al.	
	CY	US-6,049,494	04-2000	Sakui et al.	
	CZ	US-5,991,202	11-1999	Derhacopian et al.	
VTN	DA	US-5,812,457	09-1998	Arase	
	DB				
	DC				


**FOREIGN PATENT DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document Country Code <sup>3</sup> -Number <sup>4</sup> -Kind Code <sup>5</sup> (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
	DD					
	DE					
	DF					
	DG					
Examiner Signature: <i>Pho-M. Luu</i>			Date Considered: 1/7/06			



PTO/SB/08B (Substitute for form 1449/PTO)		Attorney Docket No.: 023-0031
		Application No.: 10/729,843
		First Named Inventor: Luca G. Fasoli et al.
		Filing Date: December 5, 2003
		Group Art Unit: 2824
		Examiner Name: Pho-M. Lur VTN
		Date Submitted: March 15, 2005
Sheet 1 of 2		

### NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. <sup>1</sup>	Include name of author (in CAPITAL LETTERS), title of article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
VTN	AA	DURISETY, CHANDRA SEKHAR ACHARYULU, "Analysis and Characterization of Single-Poly Floating Gate Devices in 0.35um PDSOI Process", A Thesis Presented for the Master of Science Degree, The University of Tennessee, Knoxville, December 2002, pp. i-viii and 1-80.	
	AB	EVANS, ROBERT J., ET AL., "Energy Consumption Modeling and Optimization for SRAM's," IEEE Journal of Solid-State Circuits, Vol. 30, No. 5, May 1995, pp. 571-579.	
	AC	JUNG, TAE-SUNG, ET AL., "A 117-mm <sup>2</sup> 3.3-V Only 128-Mb Multilevel NAND Flash Memory for Mass Storage Applications," IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, pp. 1575-1583.	
	AD	KAWAGOE, HIROTO, ET AL., "Minimum Size ROM Structure Compatible with Silicon-Gate E/D MOS LSI," IEEE Journal of Solid-State Circuits, Vol. SC-11, No. 3, June 1976, pp. 360-364.	
	AE	KIM, KYU-HYOUN, ET AL., "An 8-Bit-Resolution, 360-μs Write Time Nonvolatile Analog Memory Based on Differentially Balanced Constant-Tunneling-Current Scheme (DBCS)," IEEE Journal of Solid-State Circuits, Vol. 33, No. 11, November 1998, pp. 1758-1762.	
	AF	KIM, BYUNGCHEUL, ET AL., "A Scaled SONOS Single-Transistor Memory Cell for a High-Density NOR Structure with Common Source Lines," Journal of the Korean Physical Society, Vol. 41, No. 6, December 2002, pp. 945-948.	
	AG	KIM, BYUNGCHEUL, ET AL., "Single Power Supply Operated and Highly Reliable SONOS EEPROMs," Journal of the Korean Physical Society, Vol. 40, No. 4, April 2002, pp. 642-644.	
	AH	KITANO, YOSHITAKA, ET AL., "A 4-Mbit Full-Wafer ROM," IEEE Journal of Solid-State Circuits, Vol. SC-15, No. 4, August 1980, pp. 686-693.	
	AI	LEE, YONG KYU, ET AL., "Multilevel Vertical-Channel SONOS Nonvolatile Memory on SOI," IEEE Electron Device Letters, Vol. 23, No. 11, November 2002, pp. 664-666.	
	AJ	LIN, HORNG-CHIH, ET AL., "Ambipolar Schottky-Barrier TFTs," IEEE Transactions on Electron Devices, Vol. 49, No. 2, February 2002, pp. 264-270.	
	AK	NAJEEB-UD-DIN ET AL., "Analysis of Floating Body Effects in Thin Film Conventional and Single Pocket SOI MOSFETs Using the GIDL Current Technique", IEEE Electron Device Letters, Vol. 23, No. 4, April 2002, pp. 209-211.	
	AL	NISHIHARA, TOSHIYUKI, ET AL., "A Quasi-Matrix Ferroelectric Memory for Future Silicon Storage," IEEE Journal of Solid-State Circuits, Vol. 37, No. 11, November 2002, pp. 1479-1484.	
	AM	PARK, KI-TAE, "Recent Non-Volatile Memory Device & Circuit Technology," Halo LSI Inc, (date unknown), 35 pages.	
VTN	AN	ROIZIN, YAKOV, ET AL., "Plasma-Induced Charging in Two Bit per Cell SONOS Memories," Tower Semiconductor Ltd., Migdal HaEmek 23105, Israel, (date unknown), 4 pages.	
Examiner Signature			Date Considered
			1/7/06


\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	First Named Inventor: Luca G. Fasoli et al.
(Continuation Sheet)	Filing Date: December 5, 2003
	Group Art Unit: 2824
	Examiner Name: Pho-M. Luu VTN
Sheet 2 of 2	Date Submitted: March 15, 2005

**NON PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Include name of author (in CAPITAL LETTERS), title of article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
VTN	AO	SHIN, JONGSHIN, ET AL., "A New Charge Pump Without Degradation in Threshold Voltage Due to Body Effect," IEEE Journal of Solid-State Circuits, Vol. 35, No. 8, August 2000, pp. 1227-1230.	
	AP	STURM, J. C., ET AL., "Leakage Current Modeling of Series-Connected Thin Film Transistors," IEEE Transactions on Electron Devices, Vol. 42, No. 8, August 1995, pp. 1561-1563.	
	AQ	SUGIBAYASHI, TADAHICO, ET AL., "A 30-ns 256-Mb DRAM with a Multidivided Array Structure," IEEE Journal of Solid-State Circuits, Vol. 28, No. 11, November 1993, pp. 1092-1098.	
	AR	SUH, KANG-DEOG, ET AL., "A 3.3 V 32 Mb NAND Flash Memory with Incremental Step Pulse Programming Scheme," IEEE Journal of Solid-State Circuits, Vol. 30, No. 11, November 1995, pp. 1149-1156.	
	AS	TAKEUCHI, KEN, ET AL., "A Negative V <sub>th</sub> Cell Architecture for Highly Scalable, Excellently Noise-Immune, and Highly Reliable NAND Flash Memories," IEEE Journal of Solid-State Circuits, Vol. 34, No. 5, May 1999, pp. 675-684.	
VTN	AT	THEAN, AARON, ET AL., "Flash memory: towards single-electronics," IEEE Potentials, October/November 2002, pp. 35-41.	
	AU		
	AV		
	AW		
	AX		
	AY		
	AZ		
	BA		
	BB		
	BC		
	BD		
Examiner Signature		Date Considered	1/7/16

U.S. Department of Commerce, Patent and Trademark Office		Attorney Docket No.: 023-0031				
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Application No.: 10/729,843				
(Use several sheets if necessary)		Applicant(s): Luca G. Fasoli et al.				
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		Group Art Unit: 2824				
		Date Submitted: September 20, 2004				
U.S. Patent Documents						
*Examiner Initial		Document Number	Date	Name		
VTN	AA	4,646,266	24 Feb 1987	Ovshinsky et al.		
	AB	5,514,907	07 May 1996	Moshayedi		
	AC	6,005,270	21 Dec 1999	Noguchi		
	AD	6,061,270	09 May 2000	Choi		
	AE	6,163,048	19 Dec 2000	Hirose et al.		
	AF	6,420,215	16 Jul 2002	Knall et al.		
	AG	6,456,528	24 Sep 2002	Chen		
VTN	AH	US 2001/0055838 A1	27 Dec 2001	Walker et al.		
	AI					
	AJ					
	AK					
Foreign Patent Documents						
				Translation		
		Document	Date	Country	Yes	No
	AL	0 528 367 A1	24 Feb 1993	Europe		
	AM	0 575 051 A1	22 Dec 1993	Europe		
	AN					
	AP					
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)						
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